(Preliminary)SE9175

2A Sink/Source Bus Termination Regulator

General Description

The SE9175 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage cab be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The SE9175 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The SE9175 are available in the PSOP-8 (Exposed Pad) surface mount packages.

Features

- Ideal for DDR-I, DDR-II and DDR-III VTT Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Voltage traces REFEN Pin Voltage.
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- Thermal Shutdown Protection
- PSOP-8 with exposed pad Pb-Free Package.

Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems